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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/769,534	AKIYOSHI, HIDEO	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-11,14,16,18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,6,10,11,14,16,18 and 20* is/are allowed.

6)☒ Claim(s) *1,7-9 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted Feb 4, 2004 has been reviewed and considered with the following results:

Amended claims 11 and 14 overcame their respective objections described in the previous Office Action. Although those objections have now been withdrawn, some of the amended claims created new objections, which are described later under the appropriate section.

The cancellation of claims 2, 5, 12, 15, and 17 rendered their respective rejections moot.

Amended claims 1, 6-8, 10, 11, 16, 18, and 20 overcame the rejections of claims 1, 6-11, 16, 18, and 20 under 35 U.S.C. 112. Those rejections have been withdrawn.

The amended claims have also overcome the following prior art rejections as described in the previous Office Action: 1) claims 1 and 7 under 35 U.S.C. 102(e) with respect to Zhou et al. (Zhou – 669); 2) claims 1, 7-11, and 20 under 35 U.S.C. 102(e) with respect to Ikehashi et al. (Ikehashi); and 3) claims 8, 9, 11, 18 and 20 under 35 U.S.C. 103(a) with respect to Zhou – 669. Neither the reference of Zhou – 699, nor of Ikehashi et al., show or disclose the main reset signal generator with a plurality of pulse generators as now recited within claims 1, 8, and 9, or the generation of pulses corresponding to sub power-on reset signals as now recited within claims 7-11, and 20. Therefore, those prior art rejections have been withdrawn. However, after reconsidering the amended claims, and the newly added independent claim 21, it was determined some prior art references read on some of the claims. [For example, each of amended claims 1, and 7-9 had the "rectangular pulse" related limitation deleted.] The new prior art rejections, based on the amended claims, are described later under the appropriate section.

Claim Objections

Claims 1, 6, 8, 9, 11, 16, and 21 are objected to because of the following informalities: Claim 1, "and" should be deleted from line 3. Otherwise, it would appear the phrase "and when...switch on" on lines 3-4 is an incomplete phrase. Also in claim 1, line 4 "is supply switch" is confusing. It is believed to mean --supply is switched--, which would correspond to the phrasing added to each of claims 6-11, 16, 18, and 20. It is believed the term "translation" on line 8 of claim 1 was intended to mean --transition-- (e.g. as now recited within each of amended claims 7-9, 11, 18, and 20). Otherwise, what does "translation edge" actually mean? Claim 6, line 14 "signal , and" should have the space prior to the comma deleted. Claim 8, line 8 "pulse" should be --pulses-- since it relates to corresponding sub power-on reset signals. Claim 9, line 8 should have "a" changed to --the-- since its associated "power supply" relates to "a power supply" already recited on line 4; and on line 13, "signal ;and" should be changed to --signal; and--. Claim 11, line 8 "pluses" should be --pulses--. Although claim 16 is clearly shown as being amended, it is identified as "(Original)" instead of --(Currently Amended)-- on line 1. Claim 21, line 5 should have "a" changed to --the-- since its associated "power supply" relates to "a power supply" already recited on line 3. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7-9, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Malherbe, a reference cited in at least one previous Office Action. Fig. 4 shows a plurality of sub reset signal generators 10-14,20-23,30-34 for generating a plurality of sub power-on reset signals at timings different from each other (not labeled but understood to relate to the different configurations of the sub reset signal generators) based on the detection of power supply Vcc being switched on (and ramping from ground up to its stable operating level); a main reset signal generator 15,16,24,35,36 including a plurality of pulse generators (i.e. 15,16; 24; and 35,36) for respectively generating corresponding pulses (not labeled in Fig. 4, but corresponding to signals POR1, POR2, and PORn shown in Fig. 3) on the basis of a translation (e.g. transition) edge of a corresponding sub power-on reset signal; and composite circuit OR synthesizes the pulse to generate main power-on reset signal POR, thus anticipating claim 1. Interpreting Fig. 4 (and related Fig. 3) as showing a method for initializing an integrated circuit (e.g. understood to receive signal POR), wherein 10-14, 20-23, and 30-34 generate a plurality of sub power-on reset signals (not labeled) at different timings from each other with respect to when power supply Vcc is switched on; 15,16, 24, and 35,36 respectively generating pulses (e.g. POR1, POR2, and PORn shown in Fig. 3) on the basis of a transition edge of a corresponding sub power-on reset signal; and OR synthesizes the pulses to generate main power-on reset signal POR, anticipating claim 7. Since each sub reset signal generator (i.e. 10-14; 20-23; and 30-34) includes transistors (i.e. 10,12,13; 20,22,23; and 30,31,33,34), claim 8 is anticipated. [One of ordinary skill in the art understands each transistor will have is own respective threshold value (i.e. when the transistor switches on or off), and therefore it would be understood that the respective signal of each sub reset signal generator will be on the basis of the threshold values of the respective sub reset

signal generator's transistors.] Deeming 10-14 as a first sub reset signal generator, it includes a first transistor (e.g. 12 or 13) having a first threshold value, wherein first sub power-on reset signal (applied to the input of 15) is generated on the basis of the first threshold value when power supply Vcc is switched on and detected; 20-23 can be deemed a second sub reset signal generator, and it includes a second transistor (e.g. 22 or 23) having a second threshold value, wherein second sub power-on reset signal (applied to the input of 24) is generated on the basis of the second threshold value when power supply Vcc is switched on and detected; main reset signal generator 15,16,24 includes a plurality of pulse generators 15,16 and 24 for respectively generating pulses (e.g. POR1 and POR2 in Fig. 3) on the basis of a transition edge of a corresponding first/second sub power-on reset signal; and composite circuit OR synthesizes the pulses to generate main power-on reset signal POR to anticipate claims 9 and 21.

Claims 1, 7-9, and 21 are also rejected under 35 U.S.C. 102(e) as being anticipated by Crotty, another reference cited in at least one previous Office Action. Fig. 6 shows a circuit comprising a plurality of sub reset signal generators 630,210 for generating a plurality of sub power-on reset signals VD2,VD1 at timings different from each other (e.g. see Figs. 8 and 3) based on when power supply Vc2 is switched on and detected; main reset signal generator 640,220 includes a plurality of pulse generators 640 and 220 (e.g. see Fig. 4 for a detailed example) for respectively generating pulses POR2,POR1 on the basis of a translation (transition) edge of a corresponding sub power-on reset signal; and composite circuit 640 synthesizes the pulses to generate main power-on reset signal POR. Therefore, claim 1 is anticipated. [Note: Even though pulse generators 640 and 220 are identified in the figure as filters, one of ordinary skill in the art would realize the corresponding "filter" circuits shown in Fig. 4 would provide a

pulse output signal POR1. Using Fig. 4(a) as an example, when VD1 initially goes high, signal POR1 remains high. However, after the delayed VD1 signal passes through 420 and is applied to NAND gate 410, both of the logic gate's inputs will be high, and signal POR1 will transition (or pulse) low.] Interpreting the circuitry of Crotty in another way, 630,210 generate a plurality of sub power-on reset signals VD2,VD1 at different times when power supply Vcc2 is switched on and detected; 640,220 respectively generate pulses POR2,POR1 on the basis of a transition edge of a corresponding sub power-on reset signal; and 640 synthesizes the pulses to generate main power-on reset signal POR, thus anticipating claim 7. Letting Fig. 3(a) represent first generator 210 of the plurality of sub reset signal generators 210,630, and Fig. 8(a) represent second generator 630 of generators 210,630, one of ordinary skill in the art would understand each one includes transistors having threshold values (e.g. a point when the transistor will switch on or off). Therefore, signal VD1 will be based on the threshold values of the transistors (e.g. 330 and 340 shown in Fig. 3(a)) within 210, wherein signal VD2 will be based on the threshold values of the transistors (e.g. 830 and 840 shown in Fig. 8(a)) within 630, and claim 8 is anticipated. Modifying the above rejection slightly, first sub reset signal generator 210 has first transistor 340 having a first threshold value, and second sub reset signal generator 630 has second transistor 830 having a second threshold value, wherein their respective sub power-on reset signal is based on the respective threshold value, thus anticipating claims 9 and 21.

Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al. (Zhou – 669), cited in at least the previous Office Action. Fig. 5 shows a circuit that generates a main power-on reset signal POR, and Figs. 6(A) – 6(F) show related signals/pulses. The circuit shown in Fig. 5 is understood to provide a method for initializing an integrated circuit (e.g. see 110 in

Fig. 1) by generating a plurality of sub power-on reset signals POR1,NODE A at different timings (e.g. see Figs. 6(a) and 6(B)) based on the detection of when power supply VCC is switched on (i.e. when it ramps up from ground to its stable operating level); 530 and 524-529 generate respective pulses NODE D, NODE C on the basis of a transition edge of a corresponding sub power-on reset signal (i.e. the falling edge of pulse NODE D at T5 corresponds to the falling edge of POR1 at T1; the rising edge of pulse NODE C at T4A corresponds to the rising edge of NODE A at T2); and 540,550 synthesize these pulses to generate main power-on reset signal POR. Therefore, claim 7 is anticipated.

Allowable Subject Matter

Claims 4, 6, 10, 11, 14, 16, 18, and 20 are allowable. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the main reset signal generator's pulse signal includes at least one rectangular pulse, wherein the main reset signal generator comprises a plurality of pulse generators, as recited within claims 4, 6, and 16; 2) at least one of the generated pulses is rectangular as recited within claims 10 and 11; 3) the circuit, with a sub reset signal generator, and a main reset signal generator comprising a plurality of pulse generators and a composite circuit, also includes a reset terminal for receiving an external power-on reset signal from the IC's exterior as recited within claim 14; 4) the main power-on reset signal has pulses corresponding to each of the sub power-on reset signals as recited within claim 18; and 20) the pulses are not overlapping as recited within claim 20.

However, it is suggested claims 6, 11, and 16 have their respective objection (described above) addressed/corrected to overcome inadvertent oversights (e.g. typo) .

Claims 2, 3, 5, 12, 13, 15, 17, and 19 have been cancelled.

Response to Arguments

The applicant's arguments submitted on Feb 4, 2004, with respect to the previous Office Action's prior art rejection(s) of claim(s) 1, 7-11, 18, and 20, using either the reference of Zhou et al. (i.e. U.S. Patent 6,362,669) or Ikehashi et al., have been fully considered and are persuasive. Therefore, all of those rejections have now been withdrawn as previously described. However, upon further consideration, a new ground(s) of rejection is made in view of the Zhou et al. reference, as well as the references of Malherbe and Crotty. All of these references had been cited in at least one previous Office Action. The present Office Action's rejections are based on re-interpretations of those references, and the amended changes to the claims.

Therefore, the rejections are deemed proper with respect to how the references can be interpreted as reading on the claimed limitations.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

TLE

Terry L. Englund

23 April 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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